Exhibit B

of

37 C.F.R. § 1.131 Declaration

of Michael G. West

IN FOCUS SYSTEMS, INC. View Receiving Transactions 14-MAY-02

+- Receipt Header ----------+
| Receipt Number 8921 Expected Date Packing Slip |
++- Receipt Lines ----------++
| +More+ Quantity Destination Item |
| Unit Received Type Destination Item Description [ ] |
| EACH 100 Inve -WILSONVILLE-E 758-0009-00 IC, MERLIN ASIC |
| EACH 10 Inve -WILSONVILLE-E 758-0009-00 IC, MERLIN ASIC |
| EACH 40 Inve -WILSONVILLE-N 758-0009-00 IC, MERLIN ASIC |
| |
| |
|---------- Additional Receipt Line Information ----------|
| Order Type Purchase O Order Number 781432 Order Line 2 |
| PO Shipment 1 Receipt Date 05-SEP-95 PO Release |
| Quantity Ordered 50 Routing Direct Delivery |
| Note to Receiver |
| Destination -WILSONVILLE-NPI |
| Item Description IC, MERLIN ASIC |
| Category ALL PO Revision Hazard No Notes No |
+-+- Receipt Details ----------+-+
+----------+
EDIT PICK HELP

Char Mode: Replace Page 3 Count: *3

#10

2802

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re reissue application of

Group Art Unit: 2611

Michael G. West

Application No. 09/660,435

Filed: September 8, 2001

For: **METHOD AND APPARATUS FOR AUTOMATIC PIXEL CLOCK PHASE AND FREQUENCY CORRECTION IN ANALOG TO DIGITAL VIDEO SIGNAL CONVERSION**

Examiner: Christopher C. Grant

37 C.F.R. § 1.131 DECLARATION OF ALAN L. LASNESKI

TO THE COMMISSIONER FOR PATENTS:

I, Alan L. Lasneski, declare as follows:

1. I am a Principal Engineer, Software Development, of InFocus Corporation. Beginning in August 1995, I wrote portions of the software code used to control the Merlin ASIC and tested the Merlin ASIC to verify its operation. At that time, my title was Software Engineer III. I submit this declaration to establish reduction to practice in the United States no later than November 15, 1995 of the inventions claimed in this patent application. To do so, I attach Exhibits A and B as evidence.

2. Exhibit A is a two-page set of notes I recorded when I was first assigned to work with Michael G. West, the inventor named in this patent application, to write software code for the Merlin ASIC. The 8-15-95 entry (Ex. A, page 1) records the notes I initially took during one of my first meetings with Mr. West to learn about the Merlin ASIC programming project. The 8-31-95 entry (Ex. A, page 2) records my work writing software code to implement certain functions of the Merlin ASIC before we took delivery of it. September 5, 1995 was the date of delivery of the Merlin

ASIC to our shipping and receiving department. These 8-31-95 notes reveal that, before the Merlin ASIC was delivered, I had set up the phase-locked loop (PLL) integrated circuit to deliver clock signals to the Merlin ASIC and had begun to write low level access routines to communicate with (*i.e.*, to write data into and read data out of) the Merlin ASIC.

3. Exhibit B is a copy of pages 1-12 of my engineering notebook, in which I recorded my programming efforts to cause the Merlin ASIC to operate as intended.

4. The 10-26-95 entry (Ex. B, pages 1-4) records my preparation for laboratory work on the Merlin ASIC for mode detection, which seeks to find from a pixel resolution mode table the closest mode before beginning an iterative process of auto-tracking synchronization. This entry indicates that the low level access routines had been completed at that time. The references to "inputs" and "outputs" in Ex. B, pages 2 and 4 indicate, respectively, writing data into and reading data from the Merlin ASIC.

5. The 11-8[-95] entry (Ex. B, pages 5-7) records my preparation for laboratory work on the Merlin ASIC for implementing auto-tracking and auto-phase algorithms. The 13-day notebook interval from October 26 to November 8, 1995 represents the time it took for me to implement with the Merlin ASIC the algorithms indicated in my October 26, 1995 notes. The reference to "Base Algorithm" and the material following it indicate my work on the auto-tracking and auto-phase algorithms. The pixel clock frequency tracking equations, which determine the pixel clock period, appear in Ex. B, page 6. The phase adjustment implementation appears below the pixel clock frequency tracking equations. The diagram in Ex. B, page 7 (top) indicates signal timing conditions causing potential problem occurrences, and the diagram in Ex. B, page 7 (bottom) depicts auto-tracking of an image. The references to "expected width" and "actual width" indicate the parameters used in the iterative determination of the correct frequency and phase of the video pixel clock.

6. The 11-14-95 entry (Ex. B, pages 8-10) records my summary of what we called "pathological situations," which represent "corner cases," *i.e.*, infrequent, low probability conditions that would degrade overall system performance. The responses of the Merlin ASIC to the pathological situations were determined with the use of a Quantum video signal generator, which replicates video signals produced by different types of computers. My turning attention to the pathological situations demonstrated my satisfaction with the operation of the auto-tracking and auto-phase functions of the Merlin ASIC, on which I had worked from November 8 to November 14, 1995.

7. The 11/15/95 entry (Ex. B, pages 11 and 12) records my work "out in main," which means that I was then no longer testing the auto-tracking and auto-phase algorithms implemented in the main loop. The steps listed on Ex. B, page 11 represent status monitoring, which checks for conditions that would call for a re-run of the auto-phase algorithm. My activity on November 15, 1995 indicates I was then satisfied with the operation of the auto-tracking and auto-phase algorithms implemented in the Merlin ASIC and was at that point undertaking tasks that required monitoring of its operation.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: July 8, 2002

Alan L. Lasneski